

**Ranjeet Kumar****Specialization:** VLSI Design Embedded System**Email:** r.jcet076@gmail.com**Linkedin id :** www.linkedin.com/in/ranjeet-kumar-46259a162

Gender-Male

Contact no-8439272037

Examination	University/Institute	Year	CPI / %
M.Tech.	NIT Raipur (Chhattisgarh)	2023	8.73
B.Tech	Roorkee Institute of Technology, Roorkee (uttrakhand)	2016	68.96%
Intermediate	Woodbine Modern School, Darbhanga (Bihar)	2011	65.60%
Matriculation	Jawahar Navodaya Vidyalaya, Madhubani (Bihar)	2009	83.60%

Area of Interest

RTL/FPGA Design

Major Projects and Seminar**M.Tech Project:**

- Design of an Automatic Washing Machine using Verilog implementation (comparison of area, power, delay on 3 different virtual FPGA board.
- Power control in Device-to-Device Networks using Deep Reinforcement Learning (DQN)

Internship**Signion System Pvt. Ltd. (9-Month)**

- Work on DSP48E2 for MAC operation.
- Performed comprehensive analysis of RF packet transmission, focusing on encryption and decryption of data packets using AES IP for secure uplink-downlink communication.
- Improved RF packet data transmission by optimizing RTL code and reducing unnecessary CDC FIFO by smart FSM code design for efficient module replication.
- Designed RTL code for LED blinking/toggling sequences, with hardware implementation on FPGA Board ZCU102.
- Developed a project utilizing BRAM memory to store and manage data, interfacing it with a FIR compiler IP for executing convolution operations with a 16-tap filter coefficient.
- Eliminated redundant .coe file (coefficient file) in a Vivado generated TCL script by TCL command.
- Developed and integrated the filter block utilizing FIR IP and Delay subblocks to process input data(I,Q) generated from matlab code.

Workshop: Training**NIELIT Calicut (C2S Programme under Meity)**

- Gained hands-on experience with the Nucleo STM32G474RE MCU.
- Mastered the configuration of GPIO pins and clock settings using the STM32Cube IDE environment.
- Developed expertise in manipulating clock frequencies using Prescaler to decrease and PLL to increase.

Courses

- Digital IC Design (N.P.T.E.L)
- Verilog HDL
- Embedded Design (NIELIT)
- Deep Learning (udemy)
- Hands-On ZYNQ: Mastering AXI4 Bus Protocol (udemy)
- System on Chip Design using VIVADO :ZYBO Z-10 (udemy)

Technical Skills

- Tools :** Xilinx Vivado , Matlab, online GDB compiler.
- Scripting Language :** Basic TCL (Xilinx Command Terminal) ,Python

Research Paper

Power Control in Device -to-Device Communications using Deep Deterministic Policy Gradient (IEEE-Conference).

Position of Responsibility

- Research assistant in DSP LAB- Electronics Department, NIT -Raipur .(2021-2023).
- Currently working as a *Subject Matter Expert* as a freelancing in “*Chegg tutoring service Pvt. Ltd*”.